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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G09G 3/20, H04N 9/31 — A2

(11) International Publication Number: WO 91/15843

(43) International Publication Date: 17 October 1991 (17.10.91)

(21) International Application Number: PCT/GB91/00552

(22) International Filing Date: 9 April 1991 (09.04.91)

(30) Priority data:
9008032.6 9 April 1990 (09.04.90) GB

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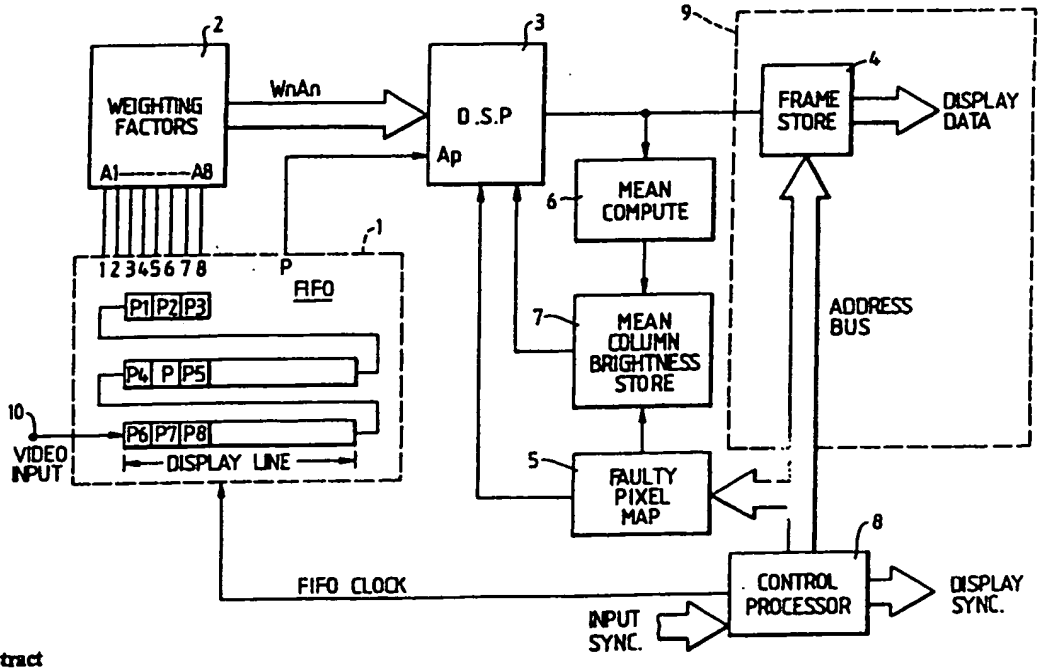
(81) Designated States: AT (European patent), AU, BE (European patent), CA, CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB, GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent), SU, US.

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: VIDEO DISPLAY SYSTEMS



(57) Abstract

A video display system of the kind which includes an active matrix having pixels which can be selectively energised is characterised in that there are means to visually compensate for a faulty pixel which either fails to light when selected or which continues to be lit when not selected, said means comprising an arrangement whereby the brightness of at least one of those pixels which are immediately adjacent the faulty pixel have their brightness automatically adjusted so that a perception of a viewer is that the faulty pixel is not in fact faulty.

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VIDEO DISPLAY SYSTEMS

The present invention relates to video display systems more particularly (but not exclusively) to projection systems, and specifically those which include a spatial light modulator device.

Spatial light modulator display devices include so-called active "active matrix" devices, in which an array of light modulating elements, or "light valves", each of which is controllable by a control signal (usually an electrical signal) to controllably reflect or transmit light in accordance with the control signal. A liquid crystal array is one example of an active matrix device; another example is the deformable mirror device (DMD) array developed by Texas Instruments and described in, for example, US4615595 or in "128 x 128 deformable mirror device" IEEE Trans. Electron Devices ED-30, 539 (1983), L J Hornbeck. One type of optical projection display using a DMD array is described in US 4680579.

Generally speaking, a DMD array comprises a plurality of separately addressed electrically deflectable mirrors; if a light beam is directed on the array device, the light reflected in a given direction by the array will depend upon the angle of inclination of each mirror, so

that a video image may be superimposed on a reflected beam of light by controlling the mirrors of the array in accordance with the values of a frame of a video signal. To produce a grey scale of intensity, it is possible to control the angle of each mirror through a continuous range using an analog control signal but a greatly preferred alternative method, which gives better contrast, involves controlling the mirror deflection between two positions corresponding to substantially reflective and unreflective states, and controlling the length of time in which the mirror in the reflective state.

Although a pulse width modulation technique could be used, as described in "Deformable Mirror Device Spatial Light Modulators and Their Applicability to Optical Neural Networks", Collins et all, Applied Optics Vol. 28, No. 22, 15 November 1989, page 4904, a preferred technique is disclosed in our United Kingdom Patent Application No. 9100188.3 filed on 4 January 1991 (agents ref. 3203201) incorporated herein by reference.

To produce a colour display, three separately illuminated active matrix devices may be provided, each controlled by a respective colour signal and illuminated

by a respective colour light beam, the modulated colour light beams being recombined for display, for example as disclosed in US4680579 or in our UK patent applications 9101715.2 and 9101714.5 filed on 25 January 1991 (agents ref. 3203301 and 3203401), incorporated herein by reference.

One example of a spatial modulator device which is not an active matrix device is the "eidophor" system, in which an oil film is illuminated by a light beam and, simultaneously, scanned by an electron beam controlled by a video signal, which acts to control the reflective state of the oil film.

Such active matrix displays include small mechanically moving components and can consequently be fragile; it is known for single pixels of the display to suffer catastrophic failure either during the manufacturing process or during service, so as to be destroyed or deactivated giving zero light output, or only an insignificantly low light output compared with that for which they were designed. Furthermore, in such active matrix displays a pixel or pixels may be electrically shorted to be permanently enabled and hence modulate light when in fact they should not be energised.

One type of active matrix display consists of an array of row and column address lines with a semiconductor device or other enabling switch at each node therebetween, the purpose of which is to select and apply data to the corresponding pixel display element according to the applied address signals.

By convention, the incoming video data is received in serial form from left to right along each display line and then line after line sequentially from the top to the bottom of the display. The received data may then be written to the pixel elements a line at a time or a frame at a time, or in any other convenient format.

Thus one may talk in terms of lines of video data or complete fields of video data. In the case of an interlaced scan display, each complete display frame of data is comprised of two separate fields of data displaced relative to each other both spatially and in time. In a progressive scanned display, the complete frame of video data is scanned in a single pass and thus a display frame is the same as a single field of video data.

It is possible to utilise this incoming video format directly by writing each item of video data to the corresponding relevant pixel display element as it arrives. Stray capacitance associated with each pixel element is utilised to store this value until the next write time (next frame), some milliseconds later.

In many instances, the incoming video data rate is such that there is insufficient time available to charge each pixel capacitance at the pixel rate time. Under these conditions, the incoming video data is first written into a temporary line store and then, at the end of each line when more time is available, the data is transferred en bloc from the line store to the relevant row of pixels. Depending on the precise implementation, the pixel write time thus available is at least equal to the line retrace time or can be as long as a complete line scan interval.

Some forms of active matrix display write the pixel data in a different format to the incoming video data and thus require the temporary storage of a complete field or frame of video data. An illustrative case in point is the matching of a progressively scanned display to an incoming interlaced video data or vice versa.

As indicated earlier there are basically two types of pixel display element fault, the first being a pixel element which fails to operate at all or fails to operate at the required light level and the second being a pixel element which remains ON when it should be OFF.

In both cases, there is a display error which is the difference between the brightness which should have been exhibited by that pixel element and the brightness it actually does exhibit.

In the case of the inoperative pixel there is no contribution to the display light output from that pixel which behaves as if it were missing.

In the case of a shorted or permanently ON pixel, the effect depends on the manner in which the device is addressed. In one type of device, successive lines of video data are applied to the column address lines, and enable signals are applied to the row lines to enable a corresponding row of switches to receive each successive line of video data as discussed in the above-cited Hornbeck paper. Each pixel retains its data for the field time interval. In such a device, a shorted pixel is permanently connected to the display column drive

line (and thus permanently enabled) and will consequently be driven by the video signal applied to every pixel element of the complete column of pixels. For an active matrix display of n lines, the video data for a pixel on any line will be present on the column line for 1/nth of the complete field time interval. Thus, a shorted pixel will display the sum of all n individual pixel contributions on that column in succession, that is the sum of each pixel brightness, each for 1/nth of a field period, as opposed to a corresponding working pixel element which displays its own value during a complete field period. Thus, the effective brightness of that pixel at any instant will correspond to the average brightness of a column of pixels containing that pixel.

The error observed is equal to the actual brightness video sample which should be displayed less this value, i.e:

$$\sum_{i=1}^{n} Pi/n - p$$

The present invention is concerned with reducing the adverse effect of faulty pixels.

According to the present invention a video display apparatus including a matrix of pixel areas corrects the video signal supplied to visually close pixel areas to oppose the effect of the error due to the faulty pixel.

In other words, the error caused by the faulty pixel is compensated by the application of a correction amount, of opposite sign and related magnitude to the error, to the surrounding display elements.

Provided that the correction signals are applied to display elements which are sufficiently close to the faulty element so that the human eye does not resolve them as separate elements of the display, a surprising reduction in the perception of the faulty pixels by a viewer may be achieved.

Other aspects of the invention will be apparent from the following description and claims.

Within the broad approach indicated in the previous paragraph the invention envisages two ways of compensating for the incorrect brightness of the faulty pixel.

The first way is to apply a correction signal continuously to all pixels in the display irrespective of whether they are faulty or not. Although correction of this kind is simple to implement because it does not require any knowledge of the location of the faulty pixel(s), it does give rise to other disadvantages. Continuous correction is accompanied by a loss of resolution. This also results in a reduction in the sharpness of the edges of any displayed objects.

Applying continuous pixel correction effectively shares the brightness of each video pixel sample between a central pixel element and it's immediately adjacent neighbours. Thus, when displaying a single bright pixel sample, the effective pixel size is increased whilst the brightness of the surrounding halo will be dependent on how the light output is split between the central element and the adjacent surrounding pixels.

There is also a blurring of the otherwise clear cut pixel edges with a consequent apparent reduction in overall display sharpness, depending on the extent of the sharing.

In situations requiring high display resolution and pixel sharpness, a second technique allowing selective correction is preferred.

This second technique involves selectively applying a correction signal to one or more of the video signal pixel samples which correspond to display pixel elements immediately adjacent the faulty pixel and not to other pixel samples.

With either method, the maximum compensation for a faulty pixel is achieved by applying the correction signal to all of those pixel samples which correspond to pixel elements immediately adjacent the faulty pixel element, and minimal compensation for a faulty pixel element would be acheived by applying the correction signal to only one of the pixel samples immediately adjacent that corresponding to the faulty pixel. For any pixel element not on the corner or edge of the display there will be eight pixel elements adjacent any other pixel in the case of a rectangular pixel

arrangement and six in the case of a diamond pixel arrangement. Therefore compensation can be achieved by applying the correction signal to between one and eight pixels adjacent a faulty pixel.

This system requires a location map of the faulty pixels. This faulty pixel map can be provided in permanent memory, such as EPROM (Erasable Programmable Read Only Memory), and/or be generated by an automatic self test routine.

The occurrence of a faulty pixel may be determined by activating each pixel in turn and then monitoring the resultant effect on the display light output.

Once a faulty pixel is detected, its location address is given by the current display address input. The address of the faulty pixel is then stored.

The equipment required to determine the location of the faulty pixels may form part of the display device, or may be a separate piece of equipment.

Thus, the faulty pixel map can then either be provided by the display manufacturer programmed into an EPROM or a similar memory device or can be updated automatically

at regular service intervals and stored in electrically alterable solid state or other rapid access memory.

With the selective correction system there is no loss of display resolution other than at the immediate location of a faulty pixel. With this method non-functioning pixels can be virtually fully corrected. However, in the case of shorted pixels elements in a row/column line addressed matrix, it is more difficult to implement the correction system. In order to do so it is necessary to have a knowledge of the brightness of the other pixels of the particular column or row (depending upon the address arrangement) in which the faulty pixel element in question is located.

The present invention is based on the appreciation that at normal viewing distances, particularly in relation to high resolution video displays such as so-called High Definition TV (HDTV), visual resolution as perceived by the eye of the viewer integrates the resultant bright halo surrounding the faulty pixel into a smooth final display brightness.

A colour projection device may, as shown in US4680579, be provided by three separate spatial modulator devices

each controlled by a respective colour video signal and illuminated by a corresponding coloured light beam.

It is a well known fact made use of in the broadcast of TV pictures that the human visual perception of colour has a much lower resolution than for monochrome images.

Thus, with a selective correction system involving three separate colour spatial modulator devices, correction need only be applied to the data written to the device containing the faulty pixel element.

In other words it is not necessary to compensate the brightness of the other colours for a faulty pixel in one colour modulator device only.

How the invention may be carried out will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1A illustrates a portion of an active matrix display showing a number of pixels in a rectangular array;

Figure 1B illustrates a portion of an active matrix

display showing a number of pixels in a diamond array;

Figure 2 is a block circuit diagram of an embodiment of the invention;

Figure 3 is a flow diagram illustrating schematically the method of operation of a further embodiment of the invention;

Figure 4 is a block diagram showing schematically the structure of the embodiment of figure 3;

Figure 5 is a flow diagram showing schematically the method of operation of the embodiment of figure 2;

Figures 6A and 6B are schematic illustrations of alternative arrangements of a store portion of the apparatus of figure 2;

Figure 7 shows schematically a method of deriving the contents of the store shown in figure 6;

Figure 8 shows schematically the general arrangement of a projection system including a spatial light modulator device of the active matrix type;

Figure 9 shows a portion of figure 8 in greater detail;

Figure 10 shows schematically the arrangement of a colour projection system;

Figure 11 shows schematically a portion of figure 8 in greater detail;

Figures 12A and 12B respectively show a plan and elevation view of a projection system in use;

Figure 13A shows schematically a detail of the array device of figure 9; and

Figure 13B shows an individual mirror element of the device of figure 13A.

Referring to figure 8, a projection system comprises a reflective screen (for example a cinema screen) B and a projector A, positioned and aligned relative to the screen so as to generate a focused image on the screen.

The projector A comprises a lamp A1, typically rated at several kilowatts for a cinema application, generating a light beam which is directed onto a planar active matrix display device A2 comprising, for example, a DMD array of 512 x 512 individual pixel mirrors. Each mirror of the display device A2 is individually connected to be addressed by an addressing circuit A3 which receives a video signal in any convenient format (for example, a serial raster scanned interlaced field format) and controls each individual mirror in accordance with the corresponding pixel signal value within the video signal.

The modulated reflected beam from the active matrix device A2 (or rather, from those pixel mirrors of the device which have been selectively activated by the address circuit A3) is directed to a projector lens system A4 which, in a conventional manner, focuses, magnifies and directs the beam onto the screen B as shown schematically in figure 9.

As shown in figure 10, in a three colour system, three separate active matrix devices A2a-A2c are provided, one driven by each of three separate colour video signals from the address circuit A3, with separate illumination arrangements A1a-A1c producing beams of the different

colours. The arrangement may be disclosed in US4680579, for example. The light reflected from the three devices A2a-A2c is combined (not shown) and supplied to the lens system A4.

In use in an auditorium, the projector A is positioned at a distance from the screen B, which is preferably of arcuate shape, the projector A being positioned on a line passing through the centre of curvature of the arc. The viewing space or auditorium lies between the projector A and the screen B as shown in figure 12a and 12b.

Referring to figure 11, one type of display device comprises a plurality of row enable lines A2d and a plurality of column enable lines A2e. The address circuit A3 comprises an input port receiving a digital video signal in an input format (for example, a conventional line scanned interlaced field format), a scan convertor circuit A3a for converting the input video signal format into one suitable for display on the device A2 and an addressing circuit A3b arranged to selectively activate corresponding pixel mirrors of the device A2 in accordance with a signal from the scan convertor circuit A3a. In a colour system of the type shown in figure 10, the scan convertor circuit receives

a composite colour video signal, for example, and generates therefrom three separate colour component video signals supplied to three separate addressing circuits A3b, one for each display device A2. A clock circuit A3c controls the timing of the address circuit A3b; in one preferred mode of operation, as discussed above, the intensity displayed by each pixel mirror is controlled by controlling the time for which that pixel mirror is deflected, and corresponding timing signals are derived from the clock A3c.

Referring to figure 13, associated with each crossing point where a particular row line and column line meet, there is provided a semiconductor switch A2f the control terminal of which is connected to, for example, a row enable line A2d. For example, as shown, the switch may comprise a field effect transistor, the gate of which is connected to a row enable line A2d. The source of the field effect transistor is connected to one of the column enable lines A2e and the drain to the deflection terminal of a deflectable mirror device, shown generally in figure 13B. Thus, each mirror device A2g will, when addressed by a row enable signal, deflect in response to the signal applied to its corresponding column enable line A2e.

Each mirror device A2g and switch A2f combination is arranged to latch the display state of the mirror device A2g until the next time the mirror device is addressed, in other words, for a field or frame period.

If, however, one of the semiconductor switches, A2f is shorted so that the pixel nearer A2g is permanently connected to the column enable line A2e, the mirror will respond once each line period rather than once each field or frame period, and will display, in succession, brightness value for every pixel mirror in its column.

Figure 1A illustrates a portion of a matrix device A2 with the pixel display elements arranged in a rectangular configuration and shows a faulty pixel element P and its immediately adjacent pixel elements P1 to P8 respectively.

Figure 1B illustrates a portion of a differently arranged matrix device A2 with the pixel display elements arranged in a triangular, or diamond, configuration where similar considerations apply except that there are only six pixel elements P1 to P8 surrounding the faulty pixel element P.

When applying compensation, the brightness signal

applied to a pixel display element, P, will be made up of that of its own video signal pixel sample plus contributions from samples of immediately adjacent pixel elements.

In the case of selective correction, these additional contributions are only provided from samples of faulty adjacent pixel display elements.

In the case of continuous correction, contributions from pixel samples corresponding to immediately adjacent will always be present.

FIRST EMBODIMENT

With continuous correction, each pixel display element displays its own brightness sample plus a correction contribution from the samples for each of the N pixels immediately surrounding it. This, for every pixel P,

$$B_p = K. \quad A_p + \sum_{n=1}^{n=N} W_n.A_n \quad \ldots\ldots(1)$$

where

B_p = corrected pixel brightness signal

A_p = input pixel brightness signal

K = normalising constant

A_n = input brightness signals of surrounding pixel element n

W_n = weighting factor from surrounding pixel element n

N = number of adjacent pixel elementsn used

In one embodiment, to avoid directional filtering, the share of pixel brightness allotted to each neighbour is equal so W_n=W=constant. For a uniform white display field, A_p=A_n. To normalise the corrected brightness B_p is also set equal A_p in order to remain within the dynamic brightness range of the display (in other words, so that the displayed brightness B_p is not caused to exceed the peak white value). Substituting these values into the above equation and carrying out the summation yields

$$K = 1 - KNxW \quad .....(2)$$

or

$$K = 1/(1+NW)$$

then $N < 8$ for a rectangular pixel matrix, fig.1a, or $N < 6$ for the matrix of fig.1b.

An alternative way of viewing this embodiment is to consider a single video signal pixel sample as being shared out or diffused into pixel elements surrounding the central pixel element to which it corresponds.

In general, for higher values of W the amount of light output retained within the central pixel element is lower. It is the light output contribution from the central pixel element that determines visible faulty pixels.

A value of W_n higher than the value K means that each pixel display element brightness B_p is more due to the pixel sample(s) associated with its neighbours than that with which it is associated, and results in the displayed pixel sample degenerating into an annular bright ring.

In the case of a missing pixel, the change in effective brightness will be determined by the value of K whilst in the case of a shorted pixel, the change in brightness

will be less than or equal to K depending on the mean column pixel brightness.

With reference to equation (1) it has already been shown above for continuous correction that, provided certain conditions as described earlier are met, a whole range of values for K and Wn described by the equation (2)

$$K = 1/(1+NW_n)$$

are possible. The two most noteworthy occur for $K = W_n$ or for $K = NxW_n$ where N is the number of adjacent pixels (<8) contributing to the correction.

If K=0.5, $W_n = 1/N$ results in 50% of the pixel light output coming from the central element and the remaining 50% from the surrounding adjacent pixels. Thus, in the event of a faulty pixel occurring, the maximum loss in light output from that pixel will be 50% of the pixel brightness whilst its effect on the light output of an adjacent pixel will not exceed 1/2XN of the maximum pixel brightness.

In the case when $W_n = 1$ and, for normalised total output $K = 1/(1+N)$ the loss in light output from any faulty

pixel element will not exceed 1/(1+N) of the maximum pixel brightness.

A special case occurs where a pixel lies at the edge or in a corner of the frame. Such an edge or corner pixel has only a limited number of neighbours; for example, in the matrix of figure 1A an edge pixel has only five neighbours and a corner pixel has only three. For such pixels, the value of N is different; it is therefore preferable to provide logic to detect when a pixel is an edge pixel or a corner pixel, and preferable correspondingly to apply different values of W_n.

Referring to figures 3 and 4, the operation and structure of a first embodiment of the invention performing such continuous correction will now be described. Referring to figure 3, the process comprises, for each pixel sample of an incoming video signal, detecting the values of neighbouring samples on the same and neighbouring lines of the video image, multiplying each sample value by a predetermined weighting factor W_n, and adding the accumulated sum to the present pixel value. For simplicity all the weighting factors W_n have the same value and consequently, for processing speed, the summation of

sample values is performed prior to the multiplication by the weighting factor W_n. The modified pixel value is then either written directly to the active matrix display or buffered in a frame store (for example, for scan conversion prior to display).

Referring to figure 4, apparatus for performing such an embodiment comprises an input 20 for receiving a digitised video signal, and a shift register circuit 22A for presenting a two-dimensional window comprising 9 contiguous pixel samples P, P1-P8. The shift register circuit 22 comprises two serially connected first-in first-out stores 22A,22B each of length 1 line of the video signal and a three stage delay line 22C coupled to the output of the second register 22B. The first three stages of the first-in first out registers 22A,22B and three stages of the delay line 22C, are tapped; the taps corresponding to the pixels P1-P8 are connected to a summation unit 24 the output of which is multiplied by a multiplier 26 by the fixed constant W_n.

The tap corresponding to the centre location P of the window is connected to be added to the output of the multiplier 26 at an adder stage 28, and the output of the adder 28 is multiplied by the constant K by a

multiplier 30. The digital arithmetic components 24-30 are conveniently provided as a single digital signal processing (DSP) device 32 such as the AT&T DSP32C device or the Texas Instruments TMSC30 device arranged to accept digital input samples and perform high speed arithmetic operations thereon.

It will readily be recognised that an analogue equivalent circuit to the embodiment of figure 4 could be provided, in which the video input 20 provides an analogue input sampled at the pixel rate, and the delay lines 22A-22C comprise analogue shift registers such as charge coupled device (CCD) registers or bucket brigade device (BBD) registers. In this case the summation and multiplying units 24,26 may comprise suitable operational amplifier components, as may the addition and multiplication units 28,30, or a DSP could be used if preceded by an analogue to digital convertor.

SECOND EMBODIMENT

An embodiment of the invention providing selective correction of faulty pixels only will now be described with reference to figures 5 and 2. In this embodiment, input 10 receives a digital video signal in line scanned format, as before, and supplies the input to a first-in, first-out (FIFO) store circuit 1 capable of holding two

complete video lines plus three extra pixels of digital video data as described above.

The pixel P of figure 1A is indicated together with its surrounding pixels P1 to P8.

The data values held in the first three pixels of each of the two lines plus the three additional pixels are tapped to provide the brightness values of a two-dimensional window section of the active matrix display as shown in figure 1. This data at the taps is routed via a weighting network 2 to a digital signal processor (DSP) 3, such as the AT&T DSP32C device or the Texas Instruments TMSC30, or to a dedicated digital arithmetic and logic circuit.

The corrected pixel brightness values are computed by the digital signal processor 3 according to the equation (1) referred to above, but in this embodiment, a weighted correction is only added from pixels known to correspond to faulty display elements as discussed below. The resulting corrected pixel values are then passed to a frame store 4 for display. The value of the constant K is set to unity, or close thereto, so that where no neighbouring pixel is faulty, the value of the pixel sample is unchanged.

In this embodiment the frame store 4 is provided with the active matrix display since it is required to convert the incoming video data format to that required to drive the display.

As indicated earlier, in those cases where the active matrix display does not in fact require a frame store for scan conversion, the output from the digital signal processor 3 can be fed directly to the active matrix display 9.

The location of any faulty display pixels is held in a faulty pixel map store unit 5. The unit 5 could employ either standard read-only-memory (ROM) devices or alternatively an erasable programmable read only memory (EPROM) could be employed.

The faulty pixel location information is then used by the digital signal processor 3 to decide whether to include the correction values into the final computed pixel brightness value.

A control processor 8 manages the complete system and serves to synchronise the various operations and also the final active matrix display to the incoming video format.

The control processor 8 provides the current address signals to the various data stores together with a FIFO clock signal.

The control processor 8 accepts the standard line and field synchronising signals provided with the incoming video data to determine the start of line and start of field timing.

The control processor 8 then generates new synchronising pulses required by the active matrix display taking into account the FIFO and computational delays.

Thus, during each frame, the control processor 8 generates a sequence of successive addresses, one at each step of the pixel clock. As data is clocked through the FIFO store circuit 1, a corresponding address at each stage is generated by the control processor and supplied to the address bus of the frame store 4; the address corresponds to that of the centre pixel P of the window within the FIFO store 1, and is consequently not the address of the pixel currently received at the input 10. The corrected pixel value calculated by the DSP 3 is therefore stored at the correct location in the frame store 4. The control processor 8 likewise supplies an address to the fault

pixel map store unit 5. This address likewise corresponds to the pixel element P currently in the centre location of the FIFO store 1.

Referring to figure 6A, each location in the faulty pixel map store unit 5 may comprise 16 bits, arranged as groups of two single bit flags for representing each of the pixel elements P1-P8 which surround the pixel P corresponding to that location; a first bit F_n acting as a flag indicating whether or not a fault exists at the neighbouring pixel N and a second bit T_n indicating, if a fault exists, whether it is an inactive pixel or an open circuit pixel fault.

The 16 bit contents of the location accessed within the faulty pixel map are supplied to the DSP 3, which accordingly determines from the fault flags F_n whether any of the neighbouring pixel elements to the pixel element P are faulty. If no neighbouring pixel elements are faulty the DSP 3 generates as output the unmodified pixel value P. If any neighbouring pixel n is determined to be faulty the DSP 3 examines the nature of the fault from the type flag T_n.

If the, or each, fault comprises an inoperative pixel element the DSP 3 multiplies the value of the corresponding pixel sample P_n obtained from the FIFO store 1 by the predetermined weighting factor W_n and adds this to the original pixel sample value A_p. The resulting corrected output is supplied to the write lines of the frame store 4.

If, on the other hand, the fault is indicated to be a short circuit fault, then a rather different type of correction is required. As indicated above, a short circuit will generally cause a pixel element of the display device to respond to video samples at element column positions corresponding to its own in each line of the frame (in other words, in all rows at its column position). Its instantaneous value, when averaged over an entire frame, is thus the average of the pixel values within its column.

It is thus necessary to derive some indicative measure of the mean intensity over the column. This calculated value represents the brightness which the pixel display element will appear to exhibit to a viewer. From this is subtracted the value A_n of the sample which corresponds to that display element, to give a measure

of the brightness error. The value of this brightness error is then multiplied by the predetermined weighting constant and added to the pixel value A_p. Thus, for example, if the shorted pixel appears brighter than it should, the error is negative and the value of surrounding pixels is correspondingly made lower to compensate this.

Although ideally, as shown, the column sum or average would be computed using the corrected values from the DSP 3, since corrections are relatively infrequent the uncorrected values could instead be used without significant loss of accuracy; apparatus 6,7 for computing an average is straightforward and could comprise, for example, an accumulating adder clocked once each line period, arranged to store a running average (7), to add (6) the present pixel value to its accumulated sum and then perform a bit shift to divide the sum by 2. Instead of this "running average" circuit, prior to being supplied to the video input 10, the signal could be buffered in a frame store and line averages calculated.

The mean value is stored in the mean column value store 7. This store holds the equivalent of one complete column of pixel data, corresponding to one mean value per column, and is circularly clocked with the FIFO store 1 to the appropriate column value to supply the DSP 3. A double buffer storage system is preferred such that whilst one store is accumulating the mean value, the other will output its data to the computational block 3.

The arrangement shown in figure 2 is a digital arrangement. However, this embodiment could also be realised in a sampled analogue arrangement in which the signal processing is carried out using charge coupled devices for the FIFO 1 and analogue multipliers and adders for the signal processing.

The store arrangement shown in figure 6A provides convenient addressing, since a location for each pixel sample value contains data on all the neighbouring pixel sample values. However, this results in considerable replication of data since data on whether a given pixel is faulty will be stored in a location corresponding to each of its eight neighbours. Whilst in many applications this is not a problem, an alternative arrangement of the store 5is shown in figure 6B. In

this alternative arrangement, the store 5 comprises a store 5a in which a pair of flags F_n,T_n described above are stored for each pixel display element, at a location in the store having an address corresponding to that location itself. The store 5a therefore needs to be only one-eighth the size of that previously described. An address counter 5b coupled to the address lines of the store 5a counts upwards to produce a sequence of addresses so that the two bit word comprising the two flags F1, T1 for the pixel P being processed by the DSP 3 is put on the data output bus of the store 5a. Coupled to the data bus of the store 5a is a circulating shift register 5c having the same structure as the FIFO store 1 or 22 (although each location in the store need only be two bits wide). The taps from the store 5c therefore provide eight two bit words each comprising the two flags F_n, T_n required by the DSP 3, and are used in the same manner.

Finally, if the pixel data rate is sufficiently slow, instead of generating a linear sequence of addresses, the addressing circuit 5b could instead calculate the addresses within the store 5a of all eight neighbouring pixels for each pixel P to be processed and perform eight read operations within each pixel clock cycle.

Referring to figure 7, one method of deriving the contents of the faulty pixel map 5 will now be disclosed. The first stage comprises the detection of inoperative pixels. A photosensor is placed in front of the display device. The display device is then illuminated, and each pixel display element is in turn activated. The output of the photosensor 8 is compared with a predetermined threshold, and when it falls below the threshold the corresponding pixel display element is indicated to be inoperative. If the store is arranged as in figure 6A, the corresponding pair of flags F_n, P_n are written to the eight neighbour locations in the faulty pixel map store 5; if it is arranged in figure 6B the flats are written to the pixel location itself.

A shorted pixel could be detected electrically, but optical detection is also possible; for instance, without applying a signal to the row lines of the display device, a signal may be applied in turn to each of the column lines of the device. If the photosensor indicates no illumination, no short circuit exists. However, if any column does give rise to illumination without a row line being enabled, a short circuit is present. To locate the row containing the short

circuit, each row line in turn may be enabled; when the photosensor output drops somewhat (indicating that only a single pixel is illuminated) the fault is detected and, as before, the corresponding fault and type flags are written to the appropriate locations in the store 5.

Since correcting a shorted pixel element requires additional, different, arithmetic processing to derive the column mean, it may be preferred only to correct for inoperative pixels or to provide separate pixel map stores 5 and processors 3 for each type of fault.

Preferably, the display system also includes means for correcting intensity variations of different display areas as disclosed in our application PCT/GB91/..... (agents ref. 3202999) having the same prior date and filing date as this application, incorporated herein by reference.

CLAIMS

1. Video display apparatus comprising a display device comprising separately actuable display areas, characterised by means for visually compensating for a faulty area of said device which either fails to be actuable to emit light when desired or which continues to be lit when not desired, said means being operable to adjust the light emitted by a neighbouring area so as to reduce the perceived visibility of the faulty area.

2. Video display apparatus according to claim 1, comprising a matrix of pixel element areas which can be selectively activated in which the adjusting means are arranged to automatically increase the perceived brightness exhibited by at least one pixel element adjacent a non-actuable faulty pixel element in the matrix in order to reduce the viewers perception of the faulty pixel element.

3. Video display apparatus according to claim 1 or 2, comprising means for receiving an input video signal comprising a plurality of sample portions each arranged to affect the value of a corresponding area of the display device, for amending the value of each said sample in dependence upon that of at least one sample

which is arranged to affect a neighbouring area of the display and for outputting the amended samples to control actuation of areas of the display.

4. Video display apparatus according to claim 3, in which the amending means comprise means for generating an output sample corresponding to said input sample and a predetermined proportion of each said neighbouring area sample.

5. Video display apparatus according to claim 4, in which the predetermined proportion is the same for each said neighbouring sample.

6. Video display apparatus according to claims 4 or 5, in which said neighbouring samples comprise those corresponding to neighbouring areas in two dimensions of said device.

7. Video display apparatus according to any one of claims 4 to 6 in which said predetermined proportion is such that, if the pixel sample and the neighbouring pixel samples all have the same value, the value of the output sample is equal to that of the pixel sample.

8. Video display apparatus according to claim 7, in

which said predetermined proportion is inversely related to the number of said neighbouring element samples.

9. Video display apparatus according to claims 7 or 8, in which the means for receiving an input signal is arranged to do so in a serial format, the means for amending comprises buffering means for deriving from said serial input data a plurality of parallel output data comprising the pixel sample and the neighbouring pixel samples, and means for jointly processing said pixel samples.

10. Video display apparatus according to claim 1, comprising means storing a reference signal indicating which, if any, areas of said display are faulty and means for selectively adjusting the perceived brightness exhibited by areas, in dependence upon said reference signal in such a way that the perceived brightness of areas which are sufficiently distant from said faulty areas to be visually resolvable therefrom are not adjusted.

11. Video display apparatus according to claim 10, in which only the brightness of areas immediately neighbouring said faulty areas in said array are adjusted.

12. Video display apparatus according to claims 10 or 11 comprising store means for storing a plurality of digital signals corresponding to areas of said array.

13. Video display apparatus according to claim 12 in which said store means comprises a plurality of locations each corresponding to a given area, each comprising data indicating whether or not a neighbouring pixel is faulty.

14. Video display apparatus according to claims 10 to 12, said areas comprising pixel elements, comprising means for receiving a video signal comprising a plurality of video pixel sampled portions each corresponding to one of said pixel elements, means for selectively amending the value of said pixel sample portions on dependence upon said reference signal, and means for outputting amended video signal pixel sample portions to effect the actuation of said pixel elements.

15. Video display apparatus as claimed in any one of claims 10 to 14 adapted to display an image in colour using means generating three optical image signals in three colours using three corresponding colour channel devices, means being provided to compensate only one

colour of three in the event of a faulty pixel element in one colour channel device only..

16. Video display apparatus according to claim 1, the device comprising an array of pixel display element areas, so constructed that failure of a pixel display element can cause the perceived brightness exhibited by that pixel element to depend upon the brightness of pixel elements lying in a line including said faulty pixel element in said array, in which the compensating means comprise means responsive to the perceived brightness exhibited by said elements in said line.

17. Video display apparatus according to claim 16, in which said responsive means comprise means for receiving a video image signal comprising a plurality of video image signal pixel portions each corresponding to one of said pixel elements, means for deriving from those portions corresponding to pixel elements of the line a computed correction value and means for correcting pixel elements neighbouring any said faulty element in said array on the basis of said computed value.

18. Video display apparatus according to claim 17, in which the deriving means are arranged to compute an indication of the mean brightness of said line.

19. Video display apparatus according to any one of claims 16 to 18, in which said video signal is received in a row scan format and said line comprises a column of said matrix.

20. Video display apparatus according to any preceding claim arranged to adjust the perceived brightness of pixel elements which lie at corners or edges of said matrix differently to pixel elements which do not.

21. Video display apparatus according to any preceding claim wherein the, or each, device comprises a spatial light modulator matrix device.

22. Video display apparatus according to claim 21, in which said matrix device comprises an array of selectively deflectable mirrors.

23. Video display system substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

24. A method of correcting for faulty pixel elements of a display device comprising adding a proportion of the error between the brightness generated by said element and the brightness which should be generated by said

element when actuated in response to a given video signal sample to the video signal samples which correspond to at least one element in the region of said faulty element in said device.

25. A method according to claim 24, in which the region comprises the elements immediately adjacent the faulty element.

26. A method according to claims 24 or 25 in which similar processing is applied to all signal samples, regardless of whether or not the elements to which they correspond are, or are in the region of, faulty elements.

27. A method according to claim 24 in which only video signal samples which correspond to elements which are sufficiently close to faulty elements as to be not visually resolvable therefrom are altered.

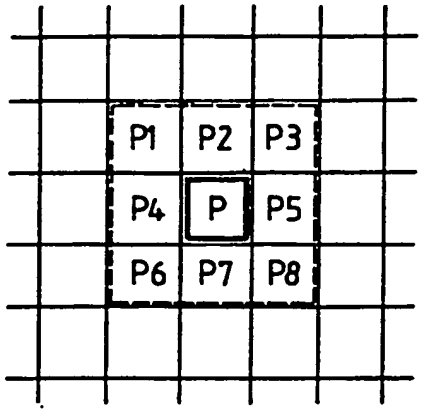
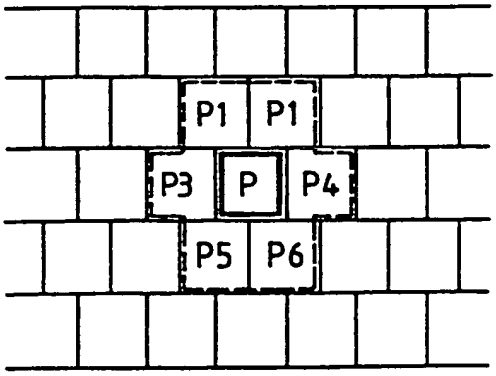


FIG. 1A

FIG. 1B



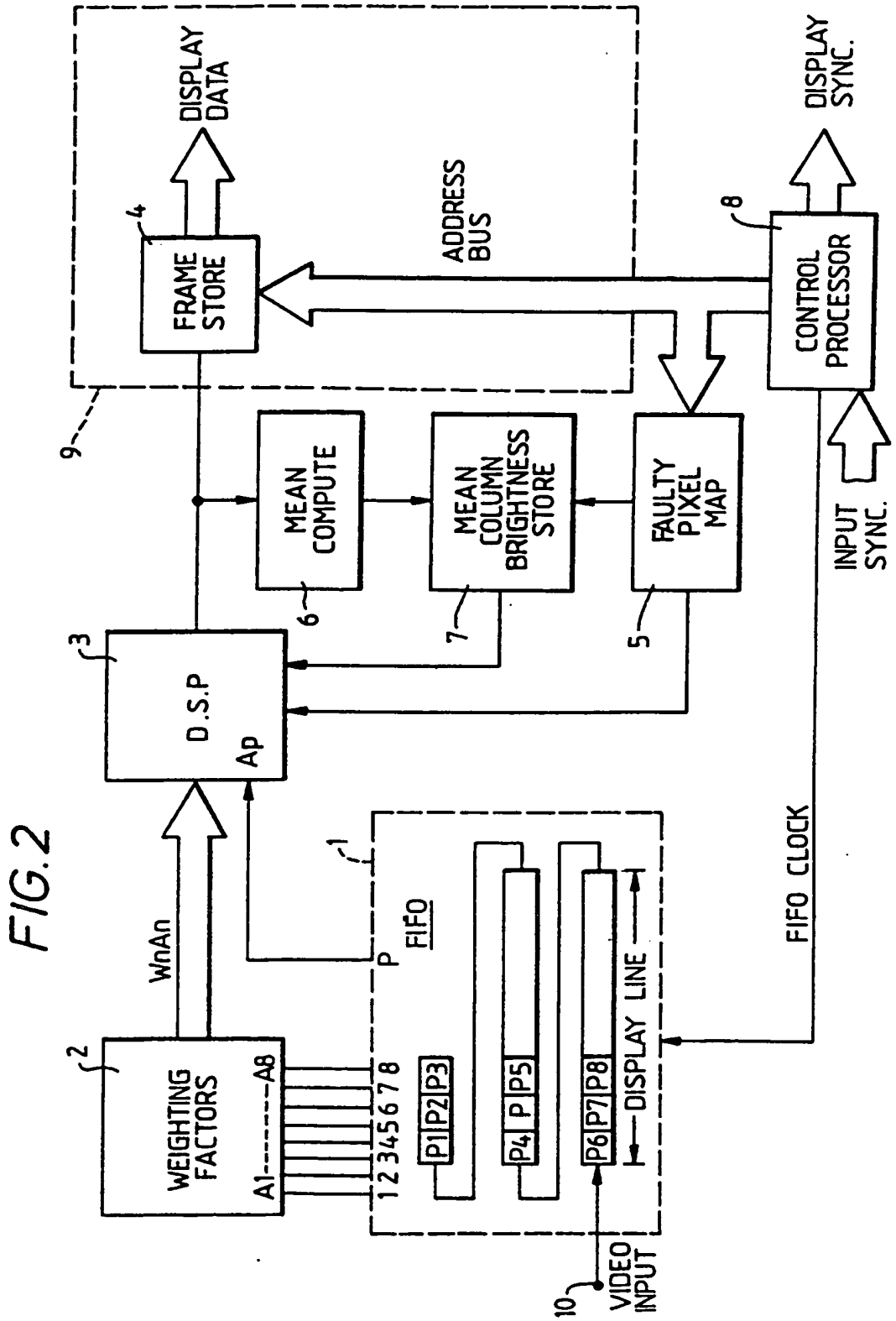

DISPLAY DATA
DISPLAY SYNC.
ADDRESS BUS
FRAME STORE
CONTROL PROCESSOR
MEAN COMPUTE
MEAN COLUMN BRIGHTNESS STORE
FAULTY PIXEL MAP
INPUT SYNC.
D.S.P
Ap
WnAn
WEIGHTING FACTORS
A1
A8
1 2 3 4 5 6 7 8
P1 P2 P3
P4 P5
P6 P7 P8
DISPLAY LINE
FIFO
P
FIFO CLOCK
VIDEO INPUT
1
2
3
4
5
6
7
8
9
10

FIG.2

FIG.3

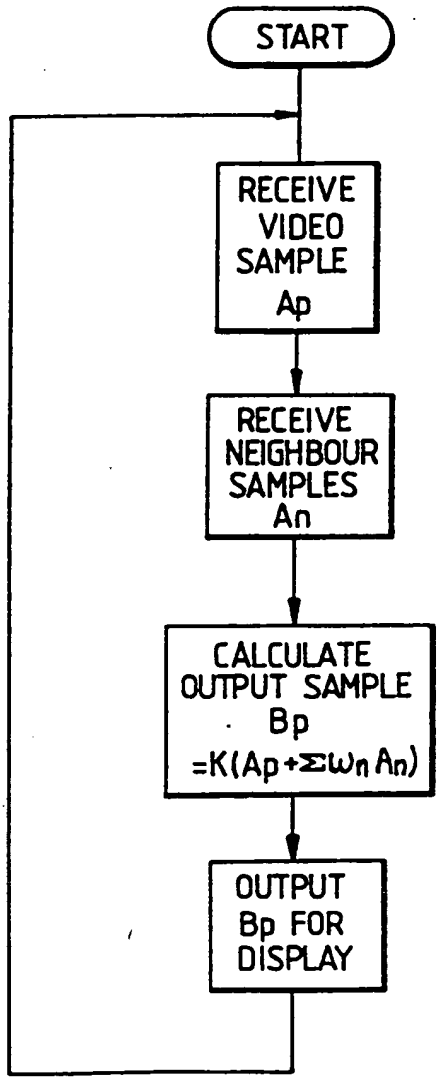
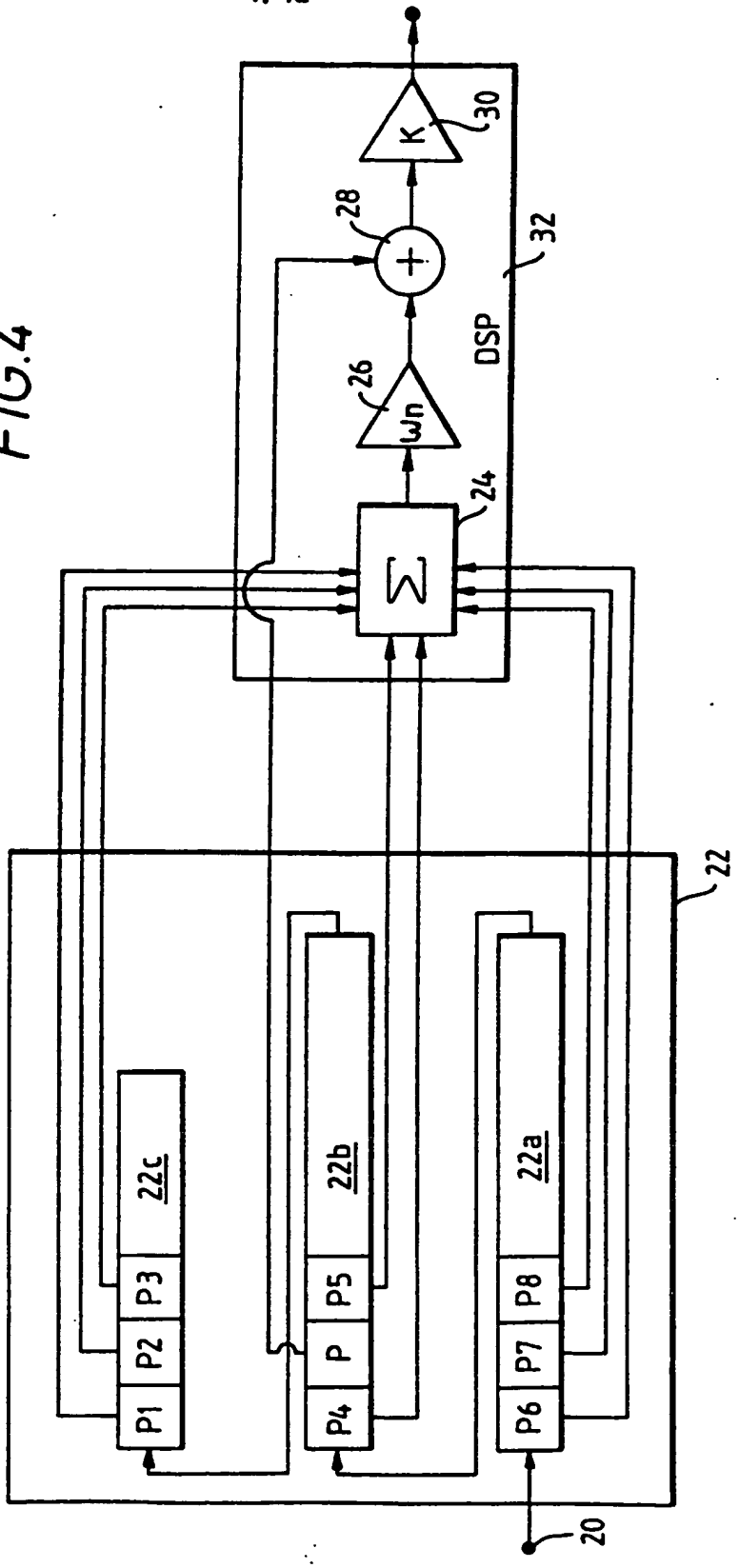

START
RECEIVE VIDEO SAMPLE Ap
RECEIVE NEIGHBOUR SAMPLES An
CALCULATE OUTPUT SAMPLE Bp =K(Ap+Σωn An)
OUTPUT Bp FOR DISPLAY

FIG.4



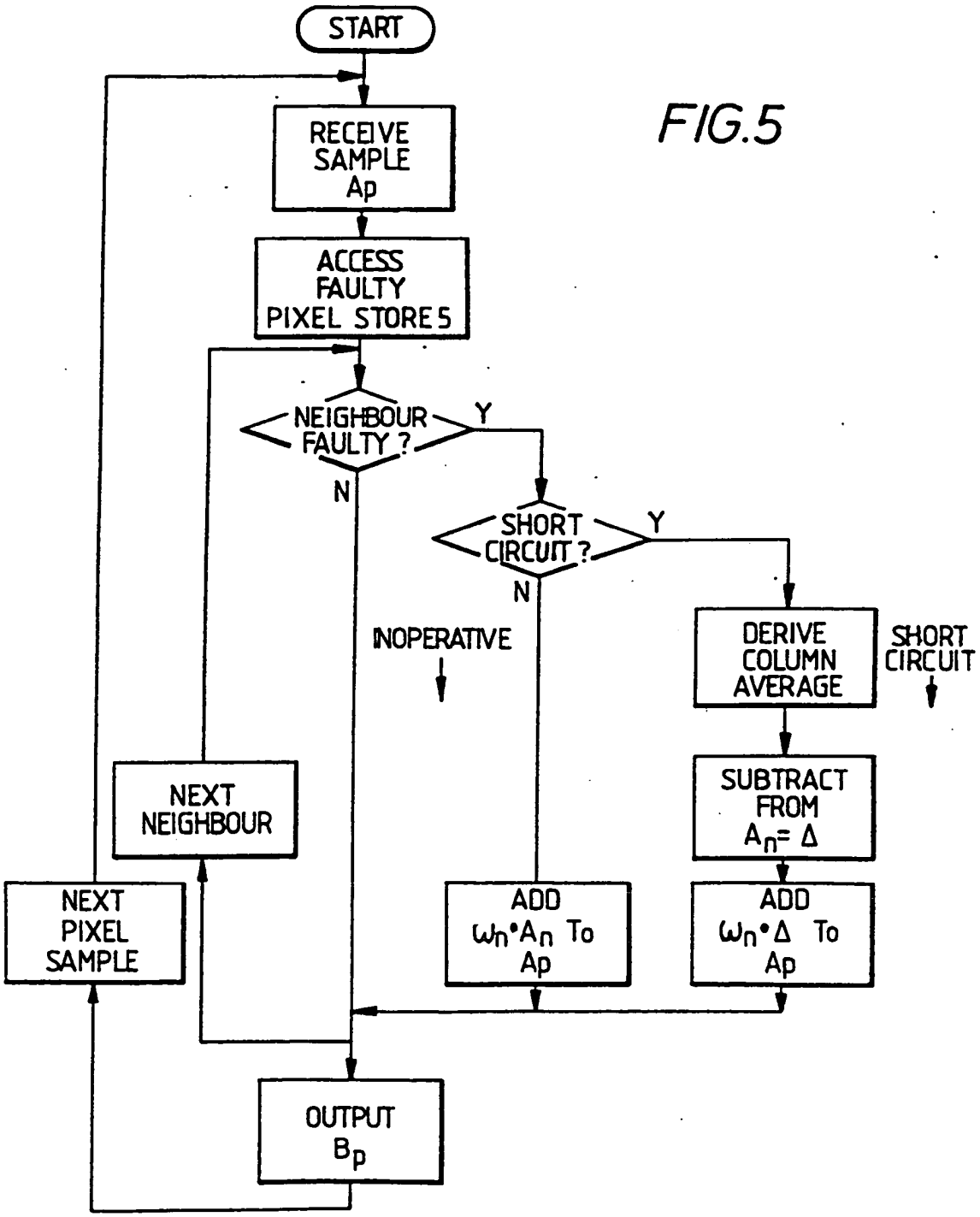

START
RECEIVE SAMPLE Ap
ACCESS FAULTY PIXEL STORE 5
NEIGHBOUR FAULTY ?
Y
N
SHORT CIRCUIT ?
Y
N
INOPERATIVE
DERIVE COLUMN AVERAGE
SHORT CIRCUIT
SUBTRACT FROM An= Δ
ADD ωn*An To Ap
ADD ωn*Δ To Ap
NEXT NEIGHBOUR
NEXT PIXEL SAMPLE
OUTPUT Bp

FIG.5

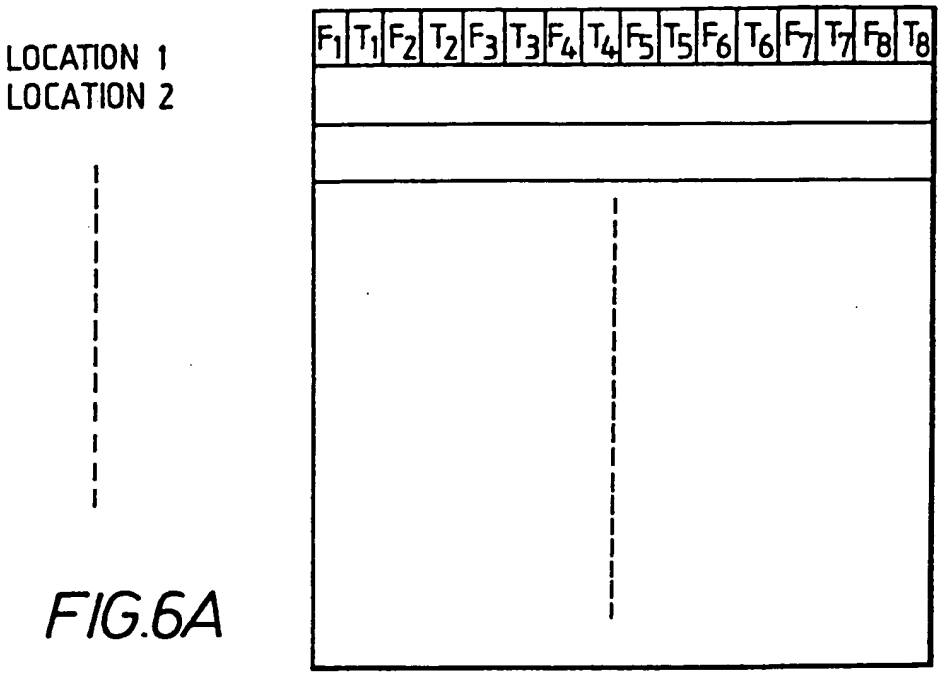

LOCATION 1
LOCATION 2
F1 T1 F2 T2 F3 T3 F4 T4 F5 T5 F6 T6 F7 T7 F8 T8

FIG.6A

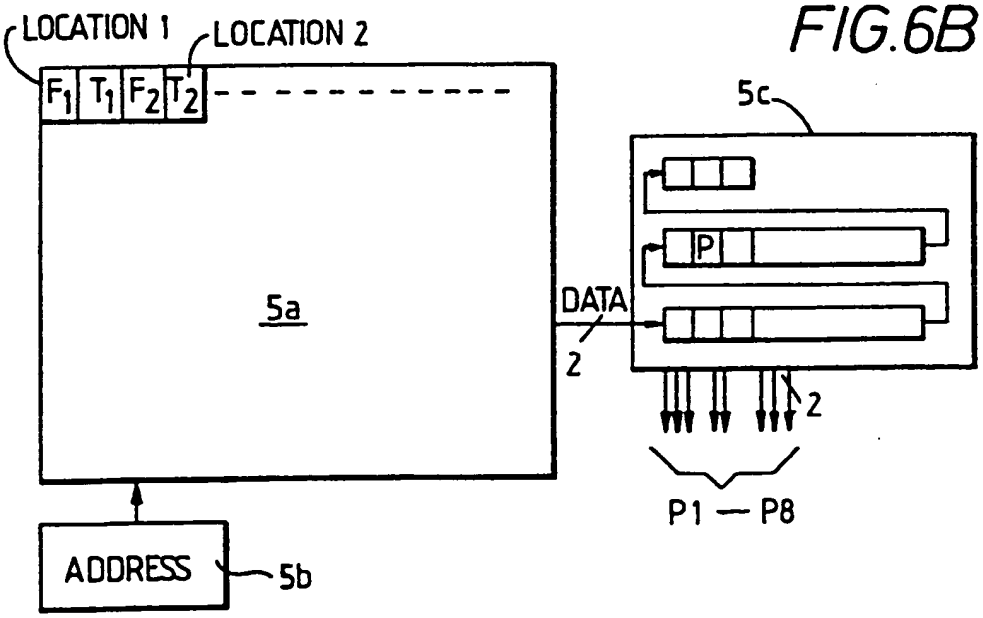
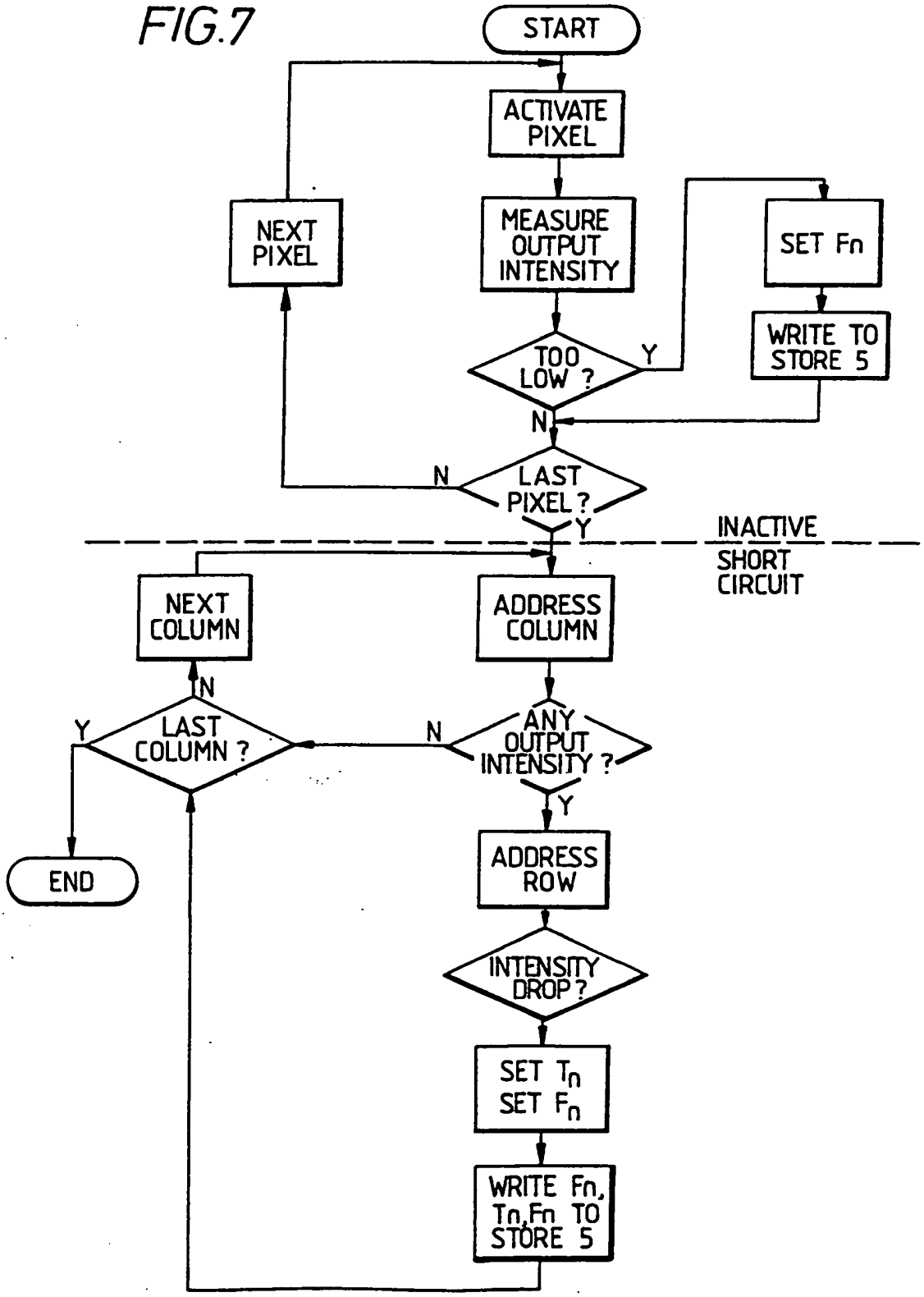

LOCATION 1
LOCATION 2
F1 T1 F2 T2
5a
5c
P
DATA
2
2
P1 — P8
ADDRESS
5b

FIG.6B

FIG.7


START
ACTIVATE PIXEL
MEASURE OUTPUT INTENSITY
TOO LOW ?
Y
SET Fn
WRITE TO STORE 5
N
NEXT PIXEL
N
LAST PIXEL ?
Y
INACTIVE
SHORT CIRCUIT
NEXT COLUMN
ADDRESS COLUMN
N
Y
LAST COLUMN ?
N
ANY OUTPUT INTENSITY ?
Y
END
ADDRESS ROW
INTENSITY DROP ?
SET Tn
SET Fn
WRITE Fn, Tn,Fn TO STORE 5

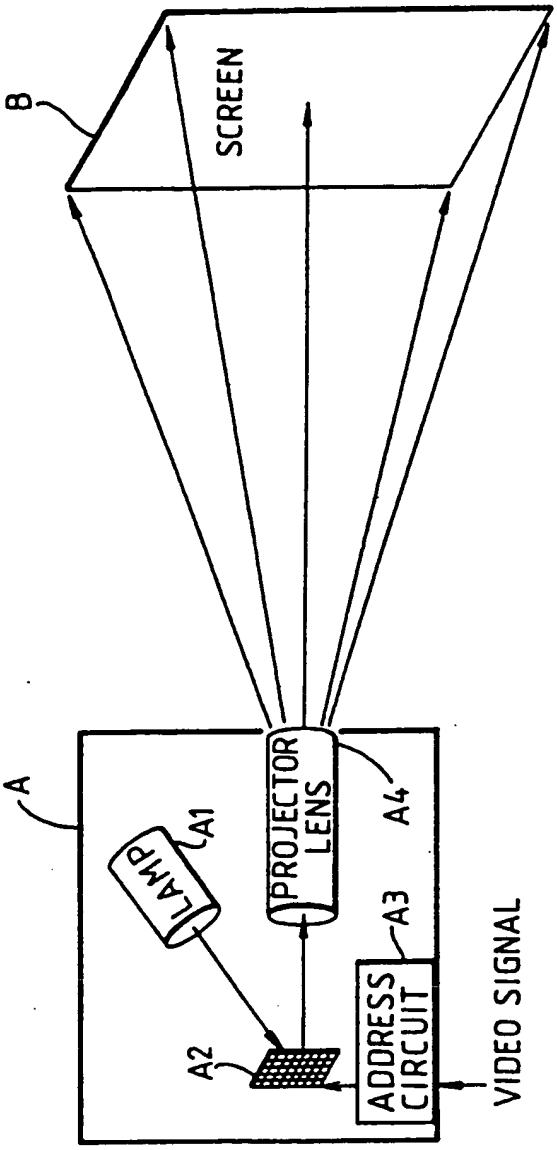

B
SCREEN
A
A1
LAMP
PROJECTOR LENS
A4
A3
ADDRESS CIRCUIT
A2
VIDEO SIGNAL

FIG.8

FIG.9

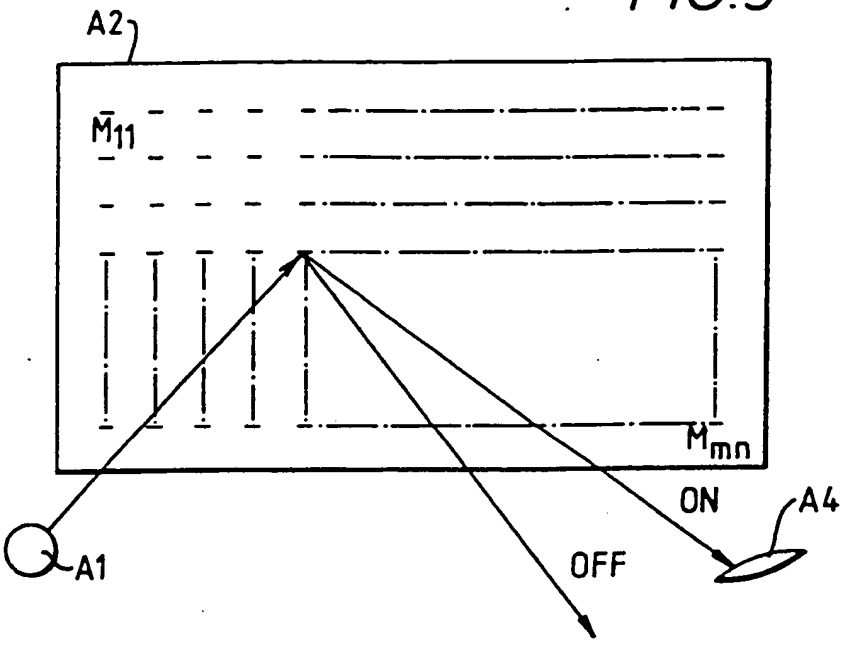
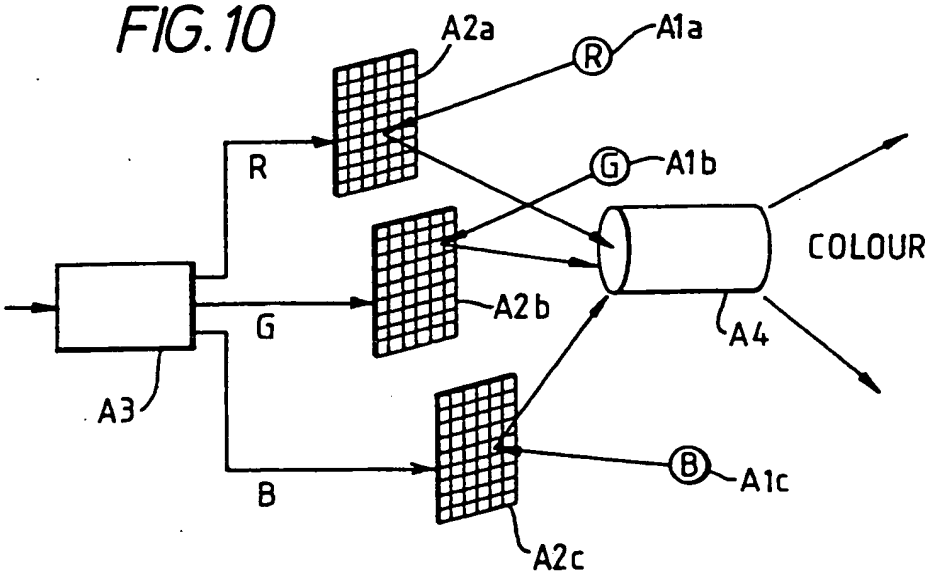

A2
M11
Mmn
ON
A4
A1
OFF

FIG.10


A2a
R
A1a
R
G
A1b
COLOUR
A2b
G
A4
A3
B
B
A1c
A2c

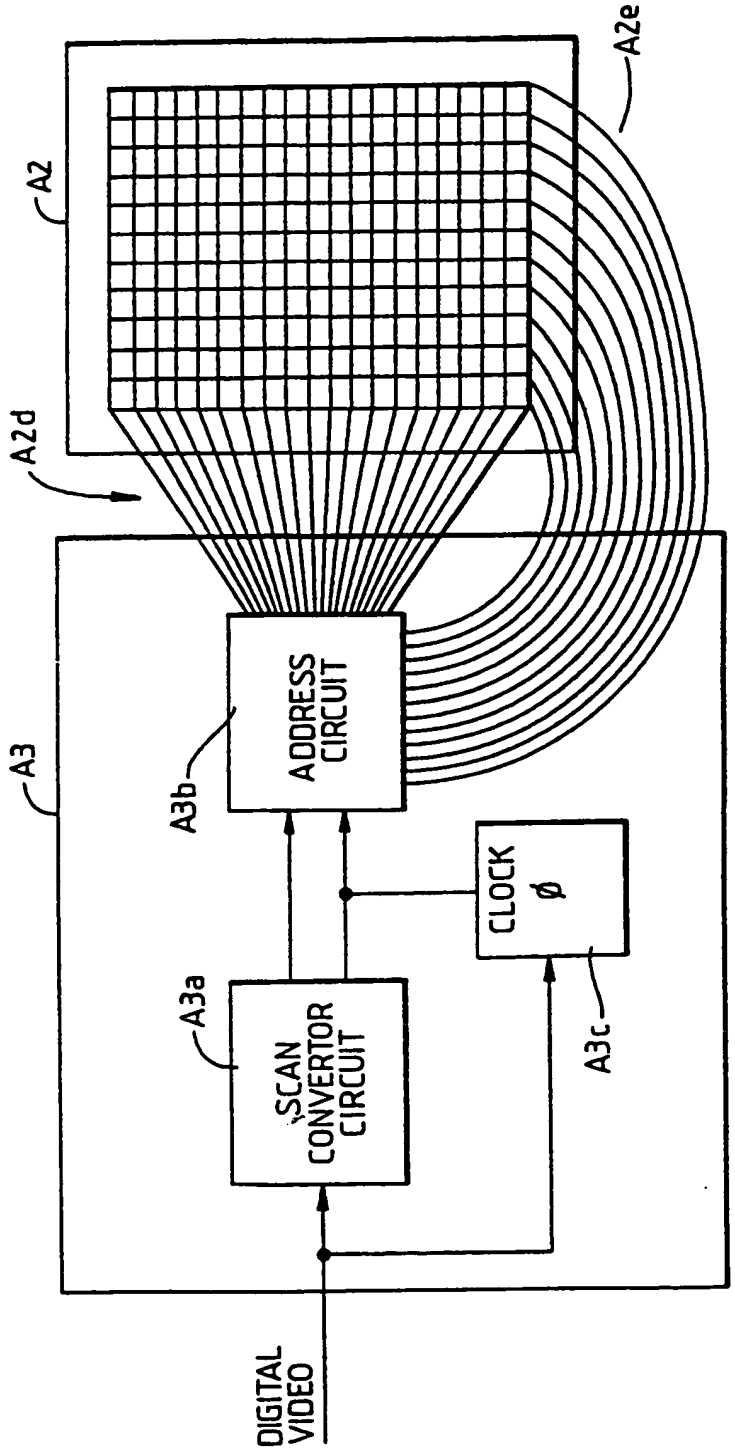

A2e
A2
A2d
A3
A3b
ADDRESS CIRCUIT
CLOCK ø
A3a
SCAN CONVERTOR CIRCUIT
A3c
DIGITAL VIDEO

FIG.11

FIG. 12A

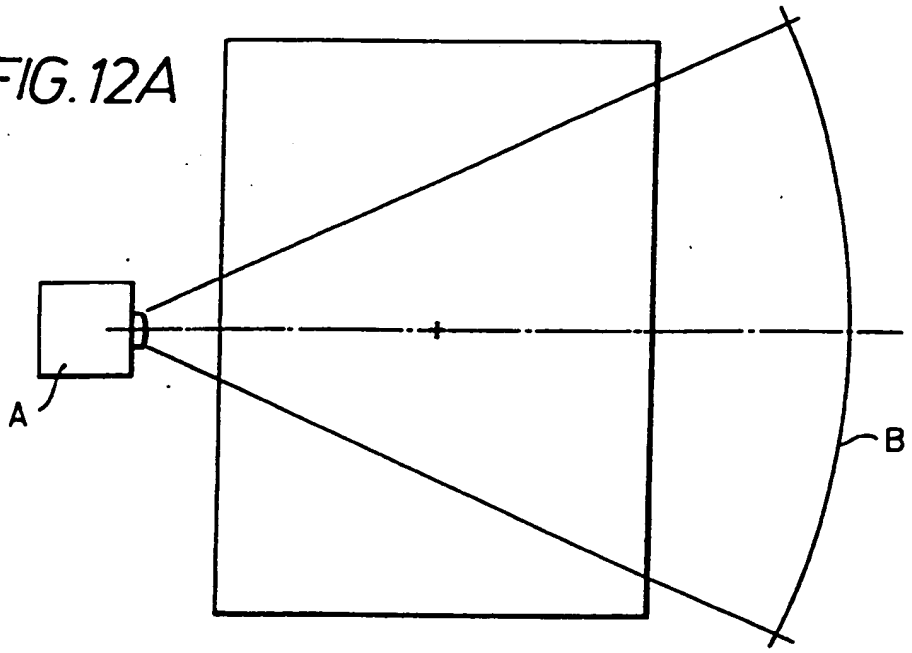


FIG. 12B

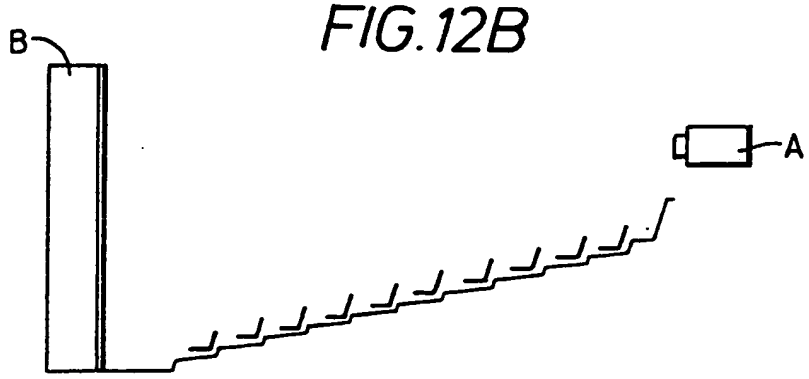


FIG. 13A

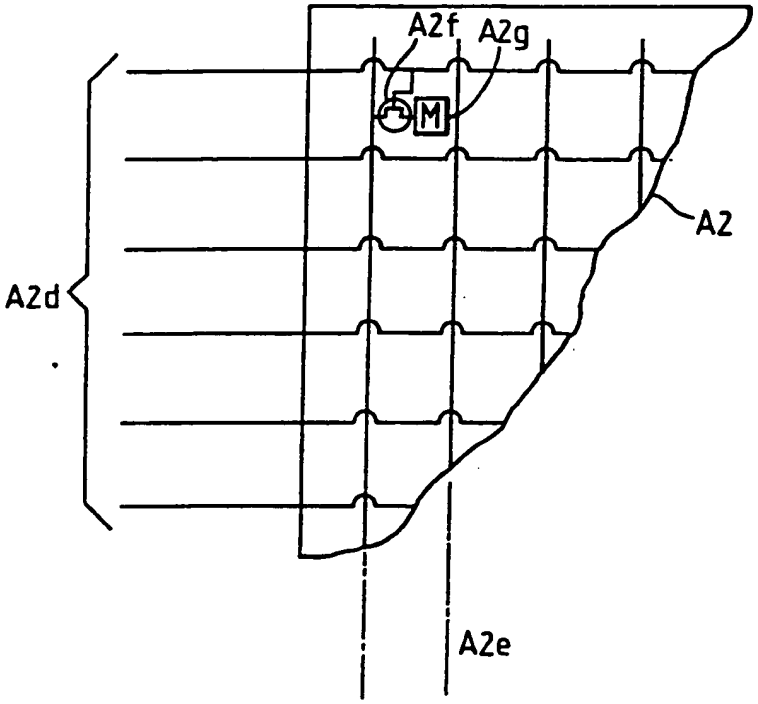
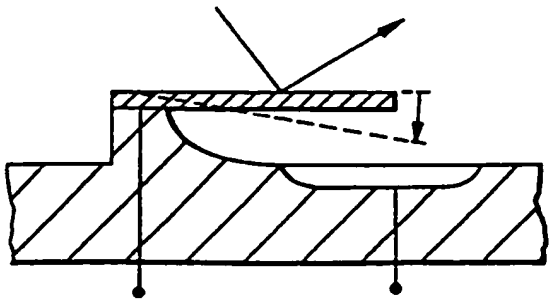



FIG. 13B